Avalanche Photodiode Bias Controller and Wide-range (5 nA – 5 mA) Current Monitor

PRELIMINARY TECHNICAL DATA

ADL5317

FEATURES

Accurately sets avalanche photodiode bias voltage
- **Wide bias range from 6 V to 75 V set**
- **Using 3V-compatible control interface**

Monitors photodiode current (5:1 ratio) over 6 decades
- **Linearity 0.5% from 10 nA to 1 mA, 1% from 5 nA to 5 mA**

Over-current protection and over-temperature shutdown

Miniature 16-lead chip scale package (LFCSP 3 mm × 3 mm)

APPLICATIONS

Optical power monitoring and biasing in APD systems

Wide dynamic range voltage sourcing and current monitoring in high-voltage systems

GENERAL DESCRIPTION

The ADL5317 is a high-voltage, wide dynamic range biasing and current monitoring device optimized for use with avalanche photodiodes. With the provision of a stable high-voltage supply up to 80 V, the bias voltage at the **VAPD** pin can be varied from 6 V to 75 V using the 3 V-compatible **VSET** pin. The current sourced from the **VAPD** pin, over a range of 5 nA to 5 mA, is accurately mirrored with an attenuation of 5 and sourced from the **IPDM** monitor output. In a typical application, the monitor output drives a current-input logarithmic amplifier to produce an output representing the optical power incident upon the photodiode. The photodiode anode may be connected to a high-speed transimpedance amplifier for the extraction of the data stream.

A signal applied at the **VSET** pin of 0.2 V to 2.5 V with respect to **COMM** is amplified by a fixed gain of 30 to produce the 6 V to 75 V bias at pin **VAPD**. The accuracy of the ADL5317's bias control interface allows for straightforward calibration to maintain constant avalanche multiplication factor of the photodiode over temperature. The current monitor output, **IPDM**, maintains its high linearity versus photodiode current over the full range of APD bias voltage. The current ratio of 5:1 remains constant as **VSET** and **VPHV** are varied.

FUNCTIONAL BLOCK DIAGRAM

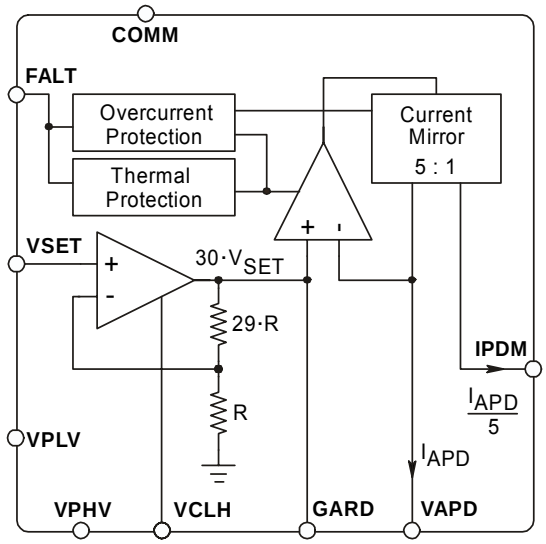

Figure 1. Functional Block Diagram

The ADL5317 also offers a supply tracking mode for compatibility with adjustable high voltage supplies. The **VAPD** pin accurately follows 2.0 V below the **VPHV** supply pin when **VSET** is tied to a voltage from 3 V to 5.5 V (or higher with current limiting resistor) and the **VCLH** pin is open.

Protection from excessive input current at **VAPD** and excessive die temperature is provided. The voltage at **VAPD** falls rapidly from its setpoint when the input current exceeds 18 mA nominally. A die temperature in excess of 140°C will cause the bias controller and monitor to shut down until the temperature falls below 120°C. Either overstress condition will trigger a logic low at the **FALT** pin, an open-collector output loaded by an external pull-up to an appropriate logic supply (1 mA max.).

The ADL5317 is available in a 16-lead LFCSP package and is specified for operation from –40°C to +85°C.

Rev. PrE

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

ADL5317—Specifications

Table 1. V_{PHV} = 78 V, V_{PLV} = 5 V, I_{APD} = 5 μA, T_A = 25°C, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
CURRENT MONITOR OUTPUT	**IPDM** (Pin 11)				
Current Gain from **VAPD** to **IPDM**	−40°C < T_A < +85°C	TBD	0.200	TBD	A/A
Nonlinearity	10 nA < I_{APD} < 1 mA		0.5	TBD	%
	5 nA < I_{APD} < 5 mA		1	TBD	%
Small-signal Bandwidth	I_{APD} = 5 nA		2		kHz
	I_{APD} = 5 μA		2		MHz
Wideband Noise at **IPDM**	I_{APD} = 5 μA, C_{GRD} = 1 nF		13		nArms
Output Voltage Range	V_{APD} > 3 V_{PLV}	0		V_{PLV}	V
	V_{APD} < 3 V_{PLV}	0		V_{APD} / 3	V
APD BIAS CONTROL	**VSET** (Pin 2), **VAPD** (Pin 8)				
Voltage Range of V_{APD}	10 V < V_{PHV} < 41 V	6		V_{PHV} −1.5	V
	41 V < V_{PHV} < 76.5 V	V_{PHV} −35		V_{PHV} −1.5	V
	76.5V < V_{PHV} < 80 V	V_{PHV} −35		75	V
Specified Input Current Range, I_{APD}	Flows from **VAPD** pin	5n		5m	A
Incremental Gain from **VSET** to **VAPD**	0.2 V < V_{SET} < 2.4 V	TBD	30	TBD	V/V
VSET Voltage Range		0.2		5.5	V
Incremental Input Resistance at **VSET**	V_{SET} = 2.0 V		50		MOhms
Input Bias Current at **VSET**	V_{SET} = 2.0 V		0.3		μA
V_{APD} Settling Time, 5%	V_{SET} = 1.6 V to 2.4 V, C_{GRD} = 1 nF		20		μsec
	V_{SET} = 2.4 V to 1.6 V, C_{GRD} = 1 nF		150		μsec
V_{APD} Supply Tracking Offset (below V_{PHV})	V_{SET} = 5.0 V, 10 V < V_{PHV} < 77 V	TBD	2.0	TBD	V
OVERSTRESS PROTECTION	**FALT** (Pin 1)				
VAPD Current Compliance Limit	V_{SET} = 2.0 V, V_{APD} deviation of 500 mV	TBD	18	TBD	mA
Thermal Shutdown Trip Point	Die temperature rising		140		°C
Thermal Hysteresis			20		°C
FALT Output Low Voltage	Fault condition, Load current < 1 mA			0.8	V
POWER SUPPLIES	**VPHV** (Pin 4, 5), **VPLV** (Pin 3)				
Low Voltage Supply	**VPLV**	4		6	V
Quiescent Current	Independent of I_{APD}		0.7	TBD	mA
High Voltage Supply	**VPHV**	10		80	V
Quiescent Current	I_{APD} = 5 μA, V_{APD} =60 V		2.0	TBD	mA
	I_{APD} = 1 mA, V_{APD} = 60 V		3.3	TBD	mA

ABSOLUTE MAXIMUM RATINGS

Table 2. ADL5317 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	80 V
Input Current at **VAPD**	25 mA
Internal Power Dissipation	615 mW
θ_{JA} (soldered exposed paddle)	65°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

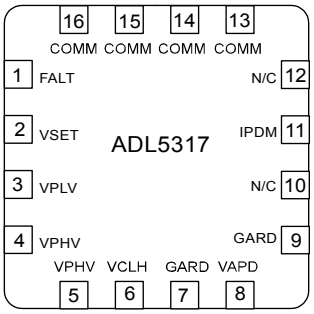

Figure 2. 16-Lead Leadframe Chip Scale Package (LFCSP)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	**FALT**	Indicates over-current or over-temperature condition. Open collector; active low.
2	**VSET**	APD Bias Voltage Setting Input. Short to **VPLV** for supply tracking mode.
3	**VPLV**	Low Voltage Supply, 4 V to 6 V
4, 5	**VPHV**	High Voltage Supply, 10 V to 80 V.
6	**VCLH**	May be shorted to **VPHV** for extended linear operating range. No connect for supply tracking mode.
7,9	**GARD**	Guard pin tracks **VAPD** pin and filters setpoint buffer noise (with extenal capacitor C_{GRD} to **COMM**). Optional shielding of **VAPD** trace. Capacitive load only.
8	**VAPD**	APD Bias Voltage Output and Current Input. Sources current only.
10	**N/C**	Optional shielding of **IPDM** trace. No connection to die.
11	**IPDM**	Photodiode Monitor Current Output. Sources current only. Current at this node is equal to $I_{APD}/5$.
12	**N/C**	Optional shielding of **IPDM** trace. No connection to die.
13–16	**COMM**	Analog Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{PHV} = 75 V, V_{APD} = 60 V, T_A = 25°C, unless otherwise noted.)

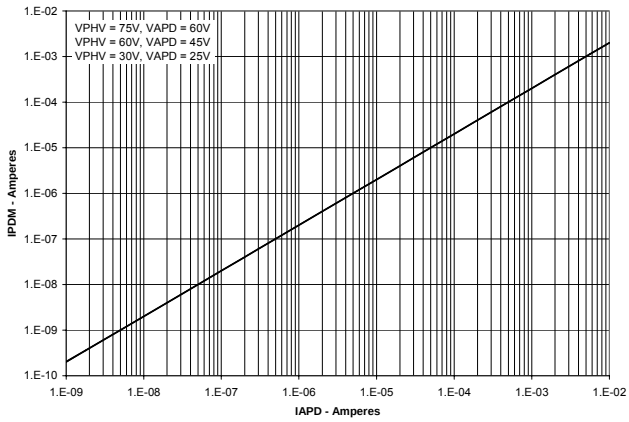

Figure 3. I_{APD} vs. I_{PDM} for Multiple Values of V_{APD} and V_{PHV}

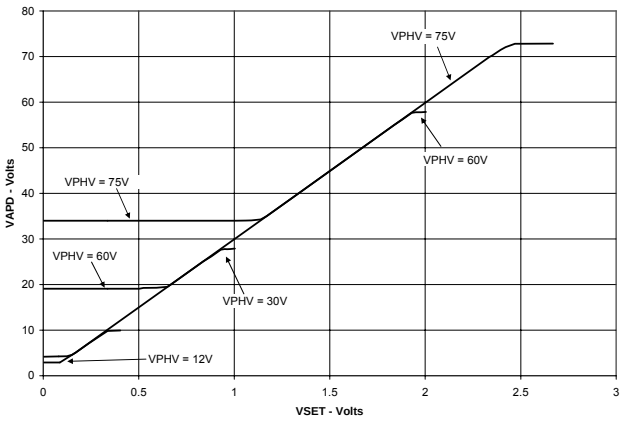

Figure 5. V_{APD} vs. V_{SET} (I_{APD} = 5 µA, VCLH open)

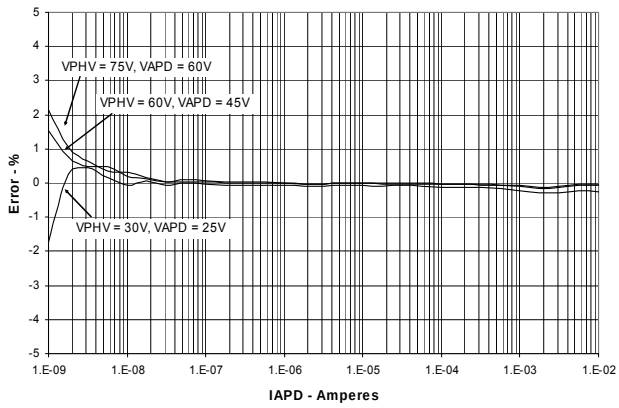

Figure 4. I_{PDM} Error vs. I_{APD} for Multiple Values of V_{APD} and V_{PHV}, Normalized to I_{APD} = 10 µA, VPHV = 75V, VAPD = 60V

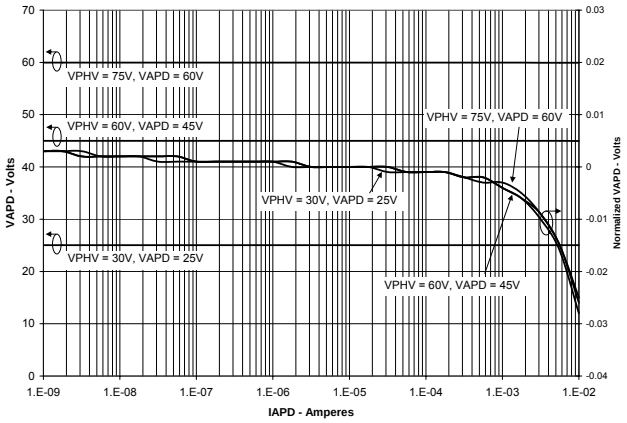

Figure 6. V_{APD} and Normalized V_{APD} vs. I_{APD} for Multiple Supply Conditions, V_{APD} Normalized to I_{APD} = 10 µA

GENERAL STRUCTURE

The ADL5317 is designed to address the need for high voltage bias control and precision optical power monitoring in optical systems utilizing avalanche photodiodes. It is optimized for use with ADI's family of translinear logarithmic amplifiers to make the best use of its wide input current range. This arrangement allows the anode of the photodiode to be connected directly to a transimpedance amplifier for the extraction of the data stream without the need for a separate optical tap for power monitoring. The basic connections for the ADL5317 are shown in Figure 7.

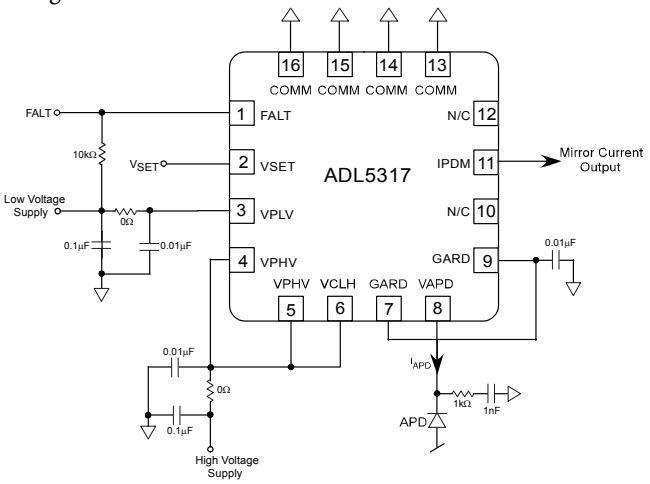

Figure 7: Basic Connections

At the heart of the ADL5317 is a precision attenuating current mirror with a voltage following characteristic that provides precision biasing at the monitor input. This architecture uses a JFET-input amplifier to drive the bipolar mirror and maintain stable VAPD voltage while offering very low leakage current at the VAPD pin. The mirror attenuates the current sourced through VAPD by a factor of 5 to limit power dissipation under high-voltage operation and delivers the mirrored current to the IPDM monitor output pin. Proprietary mirroring and cascoding techniques maintain the linearity vs. input current and stability of attenuation over a very wide range of supply and VAPD voltages.

BIAS CONTROL INTERFACE

In the linear operating mode, the voltage at VAPD is referenced to COMM, and follows the equation:

$$V_{APD} = 30 \cdot V_{SET}$$

GARD is driven to the same potential as VAPD for use in shielding the highly sensitive VAPD pin from leakage currents. The GARD and VAPD pins are clamped to within approximately 40 V below the VPHV supply to prevent internal device breakdowns, and VAPD is clamped to within a volt of GARD.

The VAPD adjustment range for a given VPHV voltage is limited to approximately 33 V (or less, for VPHV < 41 V). For example, VAPD is specified from 40 V to 73.5 V for a 75 V supply, and 6 V (the minimum allowed) to 28.5 V for a 30 V supply. When VAPD is driven to its lower clamp voltage via the VSET pin, the mirror continues to operate, but the APD bias voltage no longer responds to incremental changes in V_{SET}.

GARD INTERFACE

GARD is driven by the VSET amplifier through a 20 kΩ resistor. This resistor forms an RC network with an external capacitor from GARD to ground which filters the thermal noise of the amplifier's feedback network as well as provides additional power supply rejection. A larger value of external capacitor (up to approx. 0.01uF) will provide superior noise performance at the lowest input current levels, but will slow the response time to changes in V_{SET}. Any DC load on GARD will alter the gain from VSET to VAPD (due to the 20 kΩ source impedance). Note that the load presented by a multimeter or oscilloscope probe is sufficient to alter the VSET to VAPD gain and must be taken into account.

The GARD pin is internally clamped to approximately 40 V below VPHV to prevent device breakdown, and VAPD is clamped to within a volt of GARD. For this reason, any short circuit to ground from GARD or VAPD must be avoided for VPHV voltage above 36 V or device damage will result.

VCLH INTERFACE

The VCLH pin (Voltage CLamp High-side) is typically connected to VPHV for linear operation of the VSET interface and left open for supply tracking mode (see Applications for more details on supply tracking mode). The voltage at VCLH represents a high-side clamp above which the VSET amplifier output (and VAPD) is not allowed to rise. The voltage is internally set to a temperature-stable 2.0 V below VPHV through a 25 kΩ resistor. When V_{SET} is pulled up to 3 V or higher and VCLH is open, therefore, VAPD follows 2.0 V below VPHV as VPHV is varied. This bypasses the linear VSET interface for applications where an adjustable high-voltage supply is preferred (see Applications). The 25 kΩ source resistance allows VCLH to be shorted to VPHV, removing the 2.0 V high-side clamp for extended linear operating range (up to VPHV – 1.5 V over all conditions) in linear mode. VCLH may be left open in linear mode as well if a fixed clamp point is desired.

NOISE PERFORMANCE

Noise performance for the ADL5317 is defined as the RMS noise current as a fraction of the output DC current. The amount of noise generated by the ADL5317 improves with increasing signal current. This partially results from the relationship between quiescent collector current and shot noise in bipolar transistors. At lower signal current levels, the noise contribution from the V_{SET} amplifier and other noise sources appearing at VAPD dominate the noise behavior. Filtering the VSET interface noise through an external capacitor from GARD to ground, as well as selecting optimal external compensation components on VAPD, minimizes the amount of voltage noise at VAPD that will be converted to current noise at IPDM.

RESPONSE TIME

The response time for changes in signal current is fundamentally a function of signal current, with small-signal bandwidth increasing roughly in proportion to signal current. The value of the external compensating capacitor on VAPD strongly impacts response time; however, the value must be chosen to maintain stability and prevent noise peaking.

DEVICE PROTECTION

Thermal and over-current protection are provided with fault detection. The FALT pin is an open collector logic output (active low) designed to assert when an over-temperature or over-current condition is detected. A pull-up resistor to an appropriate logic supply is required, and its value should be chosen such that 1 mA maximum output current is used when active.

When the die temperature of the ADL5317 exceeds 140°C (typical), the current mirror will shut down, allowing VAPD to be pulled down, and FALT will assert. FALT will remain asserted until the temperature falls below the trigger temperature minus the thermal hysteresis (20°C typical), after which the mirror and biaser will again power up. The cycle may repeat until the cause of the fault is removed.

When the input current exceeds 18 mA (typical), the current mirror and biaser will attempt to maintain the threshold current by allowing the VAPD voltage to fall to a point of equilibrium. In other words, the threshold current represents the compliance of the bias voltage, in this case the current at which VAPD falls 500 mV below its mid-range current value. FALT will assert, but it is not guaranteed to remain asserted as VAPD is pulled down toward ground. If VAPD falls below ~3 V, as in the case of a momentary short circuit or being driven by a programmable current source exceeding the threshold current, bias current generators critical to device operation will become saturated, causing FALT to de-assert and the mirror to shut down. The mirror will not power up until the input current falls below the current limit of the VSET amplifier (approximately 2.5 mA), allowing VAPD to be pulled up to its normal operating level.

The FALT pin may be grounded or tied to VPLV if the logic signal is not used.

APPLICATIONS

The ADL5317 Avalanche Photodiode Bias Controller and Current Mirror is primarily designed for wide-dynamic range applications simplifying APD bias circuit architecture. Accurate control of the bias voltage across the APD becomes critical in order to maintain the proper avalanche multiplication factor as the temperature and input power vary. Figure 8 shows how the ADL5317 can be used with an external temperature sensor to monitor the ambient temperature of the APD, and then using a look-up table and DAC to drive VSET, apply the correct V_{APD} for the conditions.

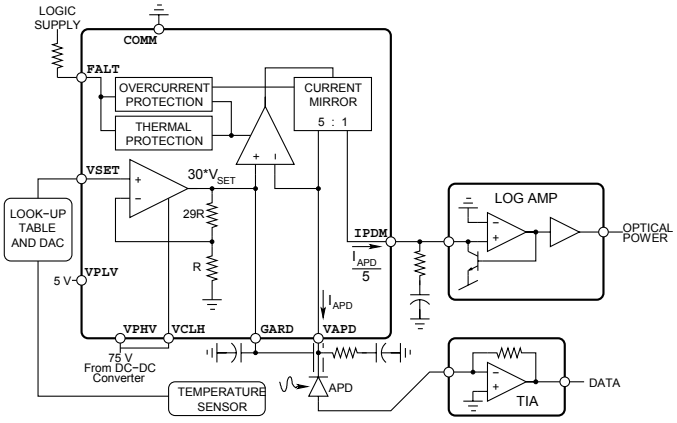

Figure 8: Typical APD Biasing Application using the ADL5317

In this application the ADL5317 is operating in it's linear mode. The bias voltage to the APD at pin VAPD is controlled by the voltage (V_{SET}) at pin VSET. The bias voltage at VAPD is equal to $30*V_{SET}$.

The range of voltages available at VAPD for a given high voltage supply is limited to approximately 33 V (or less, for VAPD < 41 V). This is because the GARD and VAPD pins are clamped to within ~40 V below VPHV, preventing internal device breakdowns

The input current I_{APD} is divided down by a factor of 5 and precisely mirrored to pin IPDM. This interface is optimized for use with any of ADI's translinear logarithmic amplifiers (AD8304, AD8305, etc.) to offer a precise, wide-dynamic range measurement of the incident optical power across the APD.

If a voltage output is preferred at IPDM a single external resistor to ground is all that is necessary to perform the conversion. Voltage compliance at IPDM is limited to VPLV.

SUPPLY TRACKING MODE

Some applications for the ADL5317 may require a variable DC-DC converter or alternative variable biasing sources to supply VPHV. For such applications it is necessary to configure the ADL5317 for Supply Tracking Mode, shown in Figure 9. In this mode the V_{SET} interfaced is bypassed, however the full functionality of the precision current mirror remains available.

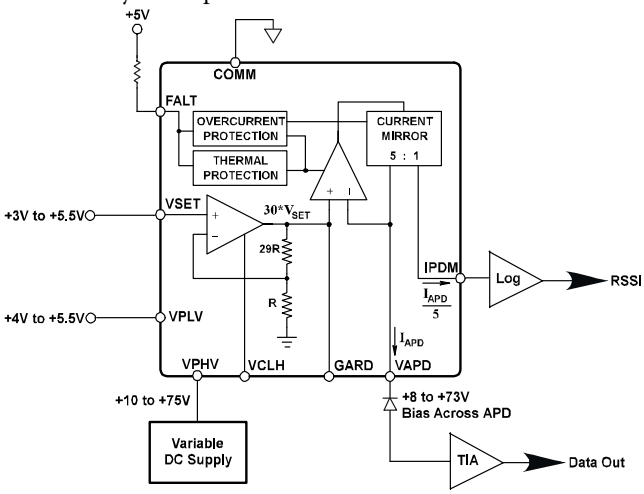

Figure 9: Supply Tracking Mode

In supply tracking mode the VSET amplifier is pulled up beyond its linear operating range and effectively placed into a controlled saturation. This is done by applying 3 V to 5.5 V at the VSET pin. It is also necessary to remove the connection from VCLH (which defines the saturation point) to VPHV. Once the ADL5317 is placed into supply tracking mode VAPD is clamped to 2.0V below VPHV.

For those designs where it is desirable to drive VSET and VPLV from the same supply it is necessary to place a 100 kΩ resistor between VSET and VPLV for voltages >5.5 V. This is due to the input current limitations on the VSET pin.

EVALUATION BOARD

Table 4: Evaluation Board Configuration Options

Component	Function	Default Condition
VPHV, VPLV, GND	**High and Low Voltage Supply and Ground Pins**	Not Applicable
VSET	**APD Bias Voltage Setting Pin.** The dc voltage applied to VSET determines the APD bias voltage at VAPD. VAPD = 30*VSET.	Not Applicable
R11, C8	**APD Input Compensation.** Provides essential HF compensation at the VAPD input pin.	C8 = 1 nF (size 0805) R11 = 1 kΩ (size 0402)
VAPD, L1, C9	**Input Interface.** The evaluation board is configured to accept an input current at the SMA connector labeled VAPD. Filtering of this current can be done using L1 and C9.	L1 = 0 Ω (size 0805) C9 = open (size 0805)
IPDM, R1	**Mirror Interface.** The output current at the SMA connector labeled IPDM is 1/5 the value at VAPD. R1 allows a resistor to be installed for applications where a scaled voltage referenced to I_{APD} is desirable instead of a current.	R1 = open (size 1206)
R7, R8, R9, R10, C6, C7, C10	**Guard Options.** By populating R9 and/or R10 the shell of the VAPD SMA connector is set to the GARD potential. R7 and R8 are installed so that the guard potential can be driven by an external source, such as the VSUM potential of Analog Devices' Optical log amps. C7 filters noise from the VSET interface as well as provides a high frequency AC path to ground. Additional filtering is possible by installing a capacitor at C10. C10 should equal C7.	R7 = R8 = 0 Ω (size 0402) R9 = R10 = open (size 0402) C7 = 0.01 µF (size 0402) C6 = C10 = open (size 0402)
VPLV, W2, R3	**Optional Supply Tracking Mode.** Connecting jumper W2 and opening W1 places the ADL5317 into supply tracking mode. In this mode the voltage at VAPD is typically 2V below VPHV. R3 = 100 kΩ for VPLV > 5.5 V.	R3 = 0 Ω (size 0402) W1 = open W2 = closed
VCLH, W1, C4, R6	**Extended Linear Operating Range.** Closing W1 connects pins VPHV and VCLH. This allows for an extended linear control range of VAPD using VSET.	W1 = closed C4 = open (size 0402) R6 = 0 Ω (size 0402)
FALT, R2	**FALT Interface.** R2 is a resistive pull-up that is used to create the logic signal at FALT.	R2 = 10 kΩ (size 0402)
C1, C2, C3, C5, R4, R5	**Supply Filtering/Decoupling**	C1 = C2 = 0.01 µF (size 0402) C3 = C5 = 0.1 µF (size 0603) R4 = R5 = 0 Ω (size 0402)

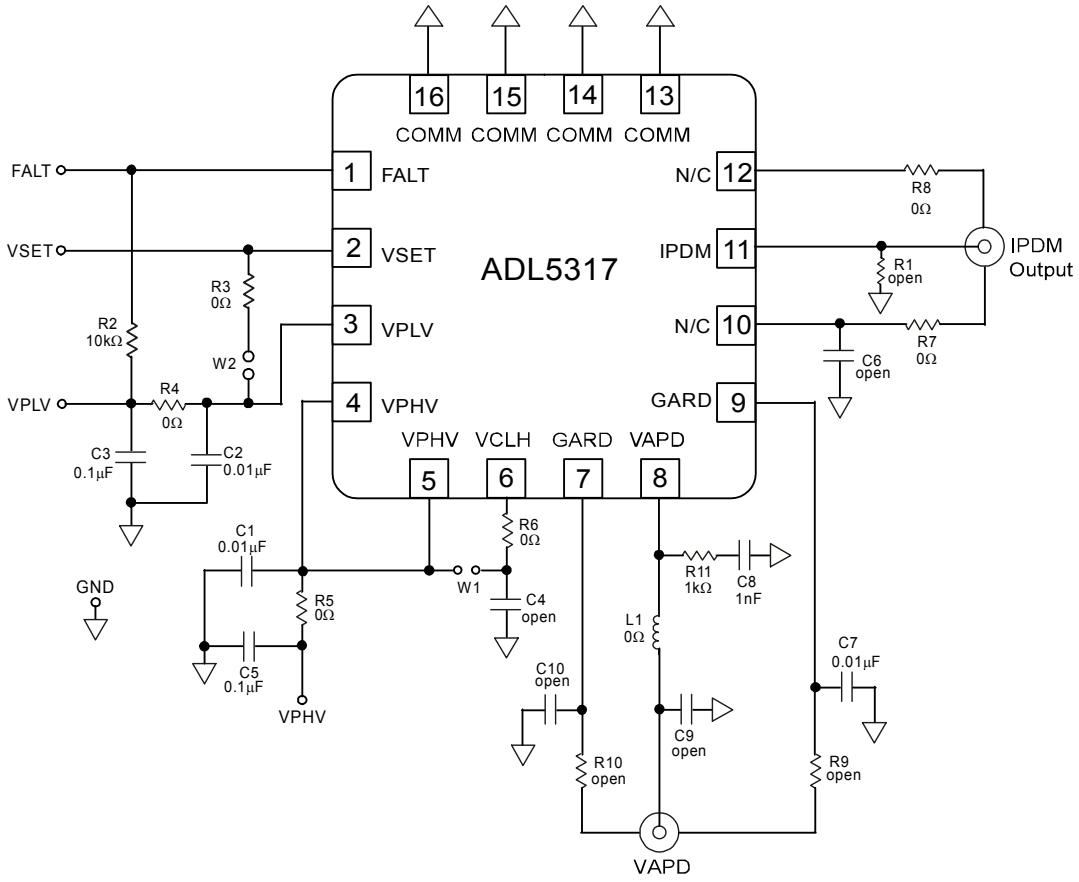

Figure 10: ADL5317 Evaluation Board Schematic

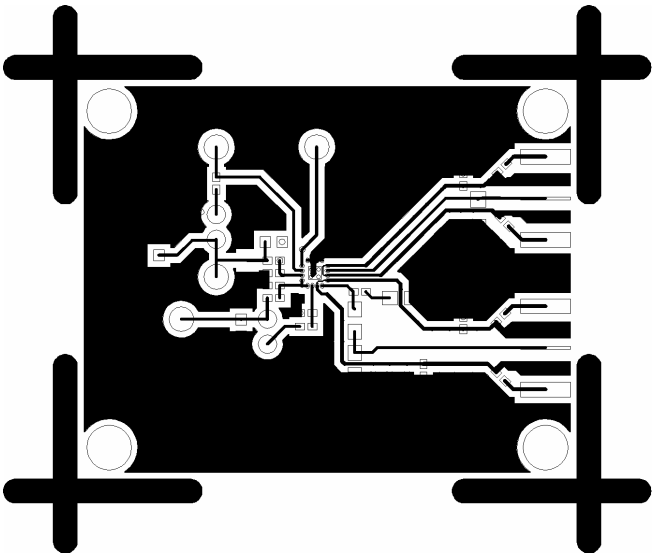

Figure 11: ADL5317 Evaluation Board Layout

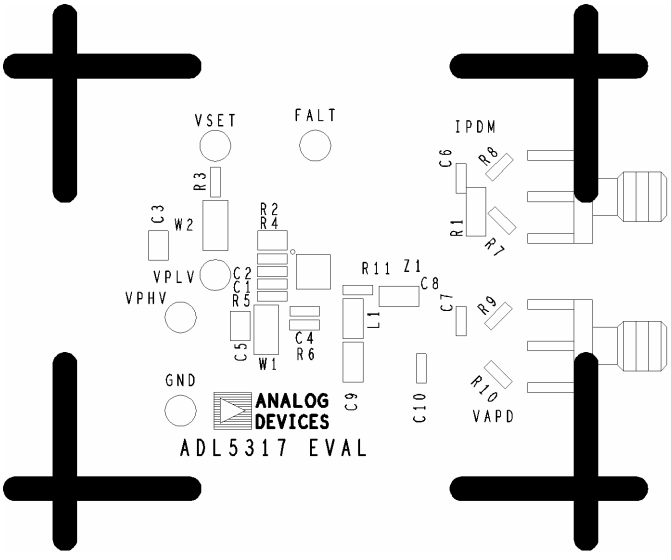

Figure 12: ADL5317 Evaluation Board Silkscreen

OUTLINE DIMENSIONS

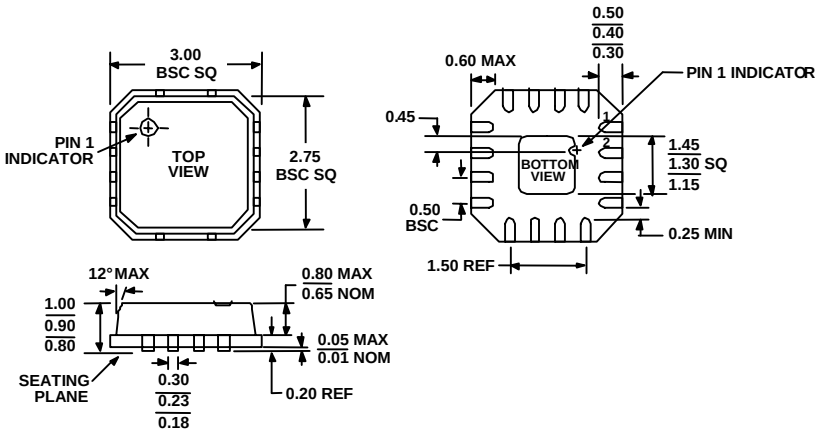

Figure 13. 16-Lead Lead Frame Chip Scale Package

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADL5317 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 5. Ordering Guide

ADL5XXX Products	Temperature Package	Package Description	Package Outline	Branding
ADL5317XCP	–40°C to +85°C	16-Lead LFCSP	CP-16	
ADL5317-EVAL		Evaluation Board		

PR05456-0-2/05(PrE)